

<b>Notice of References Cited</b>	Application/Control No. 10/678,685		Applicant(s)/Patent Under Reexamination DOUMA ET AL.	
	Examiner LINDA WONG		Art Unit 2611	Page 1 of 1

#### U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-4,276,548	06-1981	Lutz, Erno B.	342/103
*	B	US-6,275,144	08-2001	Rumbaugh, Stephen Roy	375/259
*	C	US-2004/0042504	03-2004	Khoury et al.	370/518
*	D	US-5,079,770	01-1992	Scott, Paul H.	370/536
*	E	US-2003/0195645	10-2003	Pillay et al.	700/94
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

#### FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

#### NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
*	U	Phase-Locked Loop Protocol Scheme for a Contaminated Synchronization Field. IBM Technical Disclosure Bulletin, May 1990, US Vol. No. 32, Issue 12, No. 336-337 Publication Date: May 1, 1990 (19900501)
*	V	Electronics Tutorials: Transistors, November 15, 2000, <a href="http://web.archive.org/web/20001203135600/http://www.electronics-tutorials.com/basics/transistors.htm">http://web.archive.org/web/20001203135600/http://www.electronics-tutorials.com/basics/transistors.htm</a>
*	W	
	X	

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
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